Support for claim 63 (count 1) as found in the Request for Interference:

Support for the Proposed Count 1 in the Substitute Specification to the Present Application

(N.B. All references in the right hand column are with respect to the Substitute Specification unless otherwise noted.)

Count 1	Present Application (Substitute Specification)
A non-volatile semiconductor memory device comprising:	The embodiments described are non-volatile semiconductor devices.
a plurality of bit lines;	The described memory system embodiment has a plurality of bit lines 1091, 1093, ... in Figure 12, and as described, for example, at page 28, lines 23-30.
a plurality of word lines insulatively intersecting said bit lines;	The word lines are 1077, 1079, ... in Fig. 12 and described at p. 28, lns. 18-22. These intersect the bit lines, as also shown in Figure 12. The details of this as "insulatively intersecting" can be seen in Fig. 9 and is described at p. 27, ln. 24 through p. 28, ln. 6, with an insulator, for example 1033, between word line 1027 and bit line 1019.

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion;

Fig. 12 shows the memory cell array, with cells coupled to bit lines and word lines, for example, cell 1063 coupled to 1091 and 1077. Fig. 9-11 show details of the cell with a floating gate, such as 1023, for charge storage. This is described at p. 26, ln. 29, to page 27, ln. 14.

a plurality of programming circuits coupled to said memory cell array

The programming circuits are shown in Fig. 13 as 1190, 1200, 1210, and 1220. More detail is given in Fig. 22, showing them coupled to array 1060, and in Figs. 24 and 25, showing that they are a plurality. The description is at p. 40, ln. 22 through p. 43, ln. 23.

(i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells,

This storage occurs in latch 1721 of Fig. 24, which shows in more detail block 1200 of Fig. 13, and is described at p. 41, ln. 32 through p. 43, ln. 6 in conjunction with Fig. 23.

(ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits,

Block 1210 of Fig. 13 and Fig. 22, with description at p. 41, ln. 12 through p. 42, ln. 16 in conjunction with Figs. 23 and 24.

(iii) for determining actual written states of said memory cells, and	This occurs in the compare circuit of block 1200 of Fig. 13, shown in more detail in Fig. 24 and described at p. 42, ln. 17 through p. 43, ln. 6.
(iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to achieve a predetermined written state.	Block 1210 of Fig. 13 in conjunction with blocks 1190, 1200, 1210, and 1220, as mentioned above. The program inhibit feature is described in more detail in Figs. 24 and 25 with description at p. 42, ln. 17 through p. 43, ln. 23.

The general structure of the memory array can be seen from Figure 12 of the present application as including a standard arrangement of bit lines, word lines, and memory cells. These cells are shown in detail in Figures 9-11. The description of the array is given in the disclosure from page 26, line 29 through page 29, line 21 of the Substitute Specification. This description of the cells and their arrangement is that of count 1.

The programming circuits recited in count 1 with the limitations (i)-(iv) are shown in Figure 13 as blocks 1190, 1200, 1210, 1220. Figure 22, and, particularly, Figures 24 and 25 show the relevant parts in more detail. The function of these circuits is explained at page 40, line 22 through page 43, line 23 under the general label of "Program Inhibit." It is this disclosure, along with the operation flow chart of Figure 23, that describes the programming circuit of count 1.

This is especially made clear in light of the Initial Determination by the Administrative Law Judge of the International Trade Commission ("ITC") with regard to Investigation No. 337-TA-382. This ITC proceeding resulted in claim 27 of related U.S. patent no. 5,172,338 being held valid and infringed. Sections III C and V.C. of this Initial Determination are the most pertinent to the present application, a copy of which is being filed herewith. In the present application, the numbers of the Figures are 8 higher than those of the corresponding Figures in the '338 patent, and the reference numbers are 1000 higher.

In particular, Section III.C pages 62-74 of that decision uphold the view that the present application's programming circuits are the same as those described in count 1. These pages relate to patent 5,172,338 of Mehrotra et al., the text and figures of its parent application having been incorporated into the present application by the Substitute Specification filed with the present application. The `338 patent is written to include multi-state memory, but also covers the use of binary memory cells as a simplified case. How the memory array and programming circuits described therein function, and, consequentially, relate to count 1, is described in detail in the opinion found on pages 62-74 of the ITC Initial determination. It is described more briefly here, where the references are again to the material incorporated into the present application by the earlier Preliminary Amendment.

Figure 13 is a schematic of the circuit, the memory array residing in block 1060 that is shown in more detail in figures 9-12. The programming circuits are in blocks 1190, 1200, 1210, and 1220. The compare circuit 1200 and inhibit circuit 1210 are shown in more detail in figures 24 and 25, respectively. Some comments need to made about figure 24 and its simplification in the binary memory case.

The compare circuit 1200 determines whether a memory cell is correctly programmed or not. For a binary memory cell, these two choices---correct or not---are in direct one to one correspondence with the two states of the memory cell. For a multi-state memory cell with more than two states, this one to one correspondence breaks down: one state is correct, but all the others are not. This more general (L+1) state possibility requires the L XOR gates 1711-1715 of figure 24. In the binary state

case, L=1 and there is only the single XOR gate 1711. This also reduces the NOR gate 1717 to a simple inverter for this one bit per cell case.

The one way latch 1721 then stores the data which defines whether or not write voltages are applied to the cell. This process is then done in a iterative manner until programming is complete. The read circuits 1220 of Figure 13 read out the result of an iteration, which is then compared in compare circuit 1200, and programming repeated by circuit 1210 until the circuit 1200 decides the cell is programmed. When the cell is programmed, the data bit in the one way latch 1721 is changed and, as a result, that particular cell is no longer written to. The circuit 1190 contains the initial data on which cells are to be programmed. In the multi-state case this serves as a point of reference, but can be thought of as simply a -1st iteration in the binary case of one bit per cell since there the latch 1721 determines whether the cell has achieved the predetermined state.

For these reasons, it is submitted to be clear that claim 1 of the `270 patent is supported by the present application disclosure, first filed on April 13, 1989.

Support for Claims 64-79

64. The device according to claim 63, wherein said data stored in said programming circuits are initially set to initial data, and then said initial data stored in said programming circuits are modified in accordance with said predetermined logical relationship.	This is step 3 of Figure 23 and is discussed in the Substitute Specification on page 42, lines 3-4. This is described in more detail above in the next to last paragraph of the discussion copied form the original Request for Declaration of Interference.
65. The device according to claim 64, wherein said initial data are loaded from at least one input line.	See Figure 13 with the line "LOAD PGM DATA IN" from block 170 to block 190.

66. The device according to claim 63, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.

This is described in the Substitute Specification with respect to Figure 24, beginning at page 42, line 17. In particular, see page 42, lines 26-27, "The compare circuit 1200 performs the comparison of L bits in parallel"; and beginning at line 30 of the same page: "At the same time, the N outputs such as 1725, 1727 are passed through the AND gate…".

67. The device according to claim 63, wherein said data stored in said plurality of programming circuits are modified simultaneously in accordance with said predetermined logical relationship.

This is described in the discussion of block 1200, which is shown in Figure 24, and block 1210, which is shown in Figure 25 and receives the *n* "Cells Verified" signals along 731. The discussion of Figure 24 begins on page 42, line 17, of the Substitute Specification and the discussion of Figure 25 begins on page 43, line 7, of the Substitute Specification. In particular, note beginning on line 18 of page 43: "it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This

	selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case." See also the comments related to the ITC initial determination following the support for claim 63 reproduced above from the Request for Declaration of Interference
68. The device according to claim 63, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.	The discussion for claim 67 also applies here. Concerning the "changing voltages of said bit lines...", see the discussion of claim 74 below for more detail.
69. The device according to claim 68, wherein said voltages of said bit lines are changed selectively and simultaneously by said means for selectively changing voltages of said bit lines.	See page 42, lines 10-12, of the Substitute Specification: "In figure 23(6), if any read bit fails to compare with the program data bit, a further programming voltage pulse form the program circuit is applied simultaneously to the chunk of cells.

70. The device according to claim 63, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.	This is step 5 of Figure 23.
71. The device according to claim 63, wherein modifying of said data stored in said programming circuits and applying said write voltages according to said data stored in said programming circuits are repeated during a limited number of cycles.	The write voltages are applied either until the cells program, as described with respect to claim 70, or until a preset maximum number of pulses are applied, as described in U.S. patent number 5,095,344 at column 26, lines 31-35. (U.S. patent number 5,095,344 was formerly application serial number 204,175 that is incorporated by reference into the present application on page 12, lines 12-17, and other places.)
72. The device according to claim 63, wherein said programming circuits are arranged on a semiconductor substrate.	The various elements of claim 63 are contained in 1130 of Figure 13. That these elements are arranged on a semiconductor substrate is described on page 29 of the Substitute Specification, beginning at line 25: "In the larger system, an EEprom integrated circuit chip 1130…".

73. The device according to claim 72, wherein said programming circuits are arranged adjacent to said memory cell array.

The described arrangement can be seen in Figure 13.

74. The device according to claim 63, wherein each of said programming circuits is connected to a respective one of said bit lines.

In Figure 12, the bit lines 1093, 1093, ..., are connected to V_D 1105 through the drain multiplex 1109. In Figure 13, the PROGRAM CIRCUIT WITH INHIBIT block 1210 is connected to supply a voltage to V_D along line 1105, indicated to have a width n. More detail of block 1210 is given in Figure 25 that shows the n circuits 1801 to 1803 to connect to n bit lines through 1105. Figure 25 is described beginning at page 43, line 7 of the Substitute Specification.

75. The device according to claim 63, further comprising a verify-termination detector for detecting whether or not all of said memory cells are sufficiently written in accordance with the modified data in said programming circuits based on said predetermined logical relationship.

The "verify-termination detector" is again block 1200 of Figure 13, which is shown in more detail in Figure 24.

76. The device according to claim 75, wherein said verify-termination detector is arranged on a semiconductor substrate.

Block 1200 is contained in 1130 of Figure 13. That these elements are arranged on a semiconductor substrate is described on page 29 of the Substitute Specification, beginning at line 25: "In the larger system, an EEprom integrated circuit chip 1130…".

77. The device according to claim 63, in which said plurality of programming circuits selectively modify said stored data based on said predetermined logical relationship between the determined actual written states of said memory cells after application of write voltages thereto and the actual data stored by said plurality of programming circuits prior to application of said write voltages.

These features are presented in the discussion of block 1200, which is shown in Figure 24, and block 1210, which is shown in Figure 25 and receives the *n* "Cells Verified" signals along 731. The discussion of Figure 24 begins on page 42, line 17, of the Substitute Specification and the discussion of Figure 25 begins on page 43, line 7, of the Substitute Specification. In particular, note beginning on line 18 of page 43: "it

follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case." See also the comments related to the ITC initial determination following the support for claim 63 reproduced above from the Request for Declaration of Interference.

78. The device according to claim 63, wherein said plurality of programming circuits simultaneously apply said write voltages to said part of said memory cells.

These features are presented in the discussion of block 1200, which is shown in Figure 24, and block 1210, which is shown in Figure 25 and receives the *n* "Cells Verified" signals along 731. The discussion of Figure 24 begins on page 42, line 17, of the Substitute Specification and the discussion of Figure 25 begins on page 43, line 7, of the Substitute Specification. In particular, note beginning on line 18 of page 43: "it follows that V_{PD} will be selectively passed onto those cells which are not yet verified. In this way, every time a

programming pulse is applied, it is only applied to those cells which have not yet reached their intended states. This selective programming feature is especially necessary in implementing parallel programming and on chip verification in the multi-state case." See also the comments related to the ITC initial determination following the support for claim 63 reproduced above from the Request for Declaration of Interference.

79. A non-volatile semiconductor memory device comprising: a plurality of bit lines; a plurality of word lines insulatively intersecting said bit lines; a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion; a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at	Claim 79 corresponds to claim 63 plus the additional limitations of claims 64 and 65 ("said data being initially set to initial data which are loaded from at least one input line"). Support for claim 79 is therefore given above with respect to these three claims.

least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, said write voltages applied only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

80. A system including a non-volatile semiconductor memory device comprising:

a plurality of bit lines;

a plurality of word lines insulatively intersecting said bit lines;

a memory cell array comprising a plurality of memory cells coupled to said bit lines and said word lines, each memory cell including a transistor with a charge storage portion; and

Claim 80 repeats the limitations of claim 79, but with the preamble specifying a "system including" the device of claim 79. The various limitations of claim 80 are thus supported in the application as with claim 79, with the incorporation of the device into a system shown, for example, in Figure 1A of the present application.

a plurality of programming circuits coupled to said memory cell array (i) for storing data which define whether or not write voltages are to be applied to respective of said memory cells, said data being initially set to initial data which are loaded from at least one input line, (ii) for selectively applying said write voltages to a part of said memory cells, which part is selected according to the data stored in said plurality of programming circuits, (iii) for determining actual written states of said memory cells, and (iv) for selectively modifying said stored data based on a predetermined logical relationship between the determined actual written states of said memory cells and the data stored in said plurality of programming circuits, thereby applying said write voltages only to memory cells which are not sufficiently written to produce charge storage in the charge storage portion of each respective insufficiently written memory cell.

Claims 81-91 are essentially the same as respective claims 66-76, except for tracing their dependence back to claim 80 instead of claim 63. (Claim 90 contains only part of the limitations of claim 75.) Consequently, support for the additional limitations of these claims is given above for the corresponding one of claims 66-76:

81. The system according to claim 80, wherein said plurality of programming circuits simultaneously determine said actual written states of said memory cells.	See support for claim 66 above.
82. The system according to claim 80, wherein said data stored in said programming circuits are modified simultaneously in accordance with said predetermined logical relationship.	See support for claim 67 above.
83. The system according to claim 80, wherein said programming circuits include means for selectively changing voltages of said bit lines according to said data stored in said programming circuits.	See support for claim 68 above.
84. The system according to claim 83, wherein said voltages of said bit lines are changed simultaneously by said means for selectively changing voltages of said bit lines.	See support for claim 69 above.

85. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are continued until each memory cell is sufficiently written.	See support for claim 70 above.
86. The system according to claim 80, wherein selective modifying of said data stored in said programming circuits and applying said write voltages to said respective of said memory cells are repeated during a limited number of cycles.	See support for claim 71 above.
87. The system according to claim 80, wherein said programming circuits are arranged on semiconductor substrate.	See support for claim 72 above.
88. The system according to claim 87, wherein said programming circuits are arranged adjacent to said memory cell array.	See support for claim 73 above.

89. The system according to claim 80, wherein each of said programming circuits is connected to a respective one of said bit lines.	See support for claim 74 above.
90. The system according to claim 80, further comprising a verify-termination detector for detecting whether or not all of accessed memory cells are sufficiently written.	See support for claim 75 above.
91. The system according to claim 90, wherein said verify-termination detector is arranged on a semiconductor substrate.	See support for claim 76 above.

Conclusion

A prompt consideration of the pending claims and a notice of their allowance is respectfully requested for the present application that was filed on August 5, 1998, and for which the last Office Action was mailed on July 30, 2001.

Respectfully submitted,

Michael G. Cleveland
Agent for Applicant(s)
Reg. No. 46,030

Parsons Hsue & de Runtz LLP
655 Montgomery Street
Suite 1800
San Francisco, CA 94111
(415) 318-1160
(415) 693-0194 (Fax)